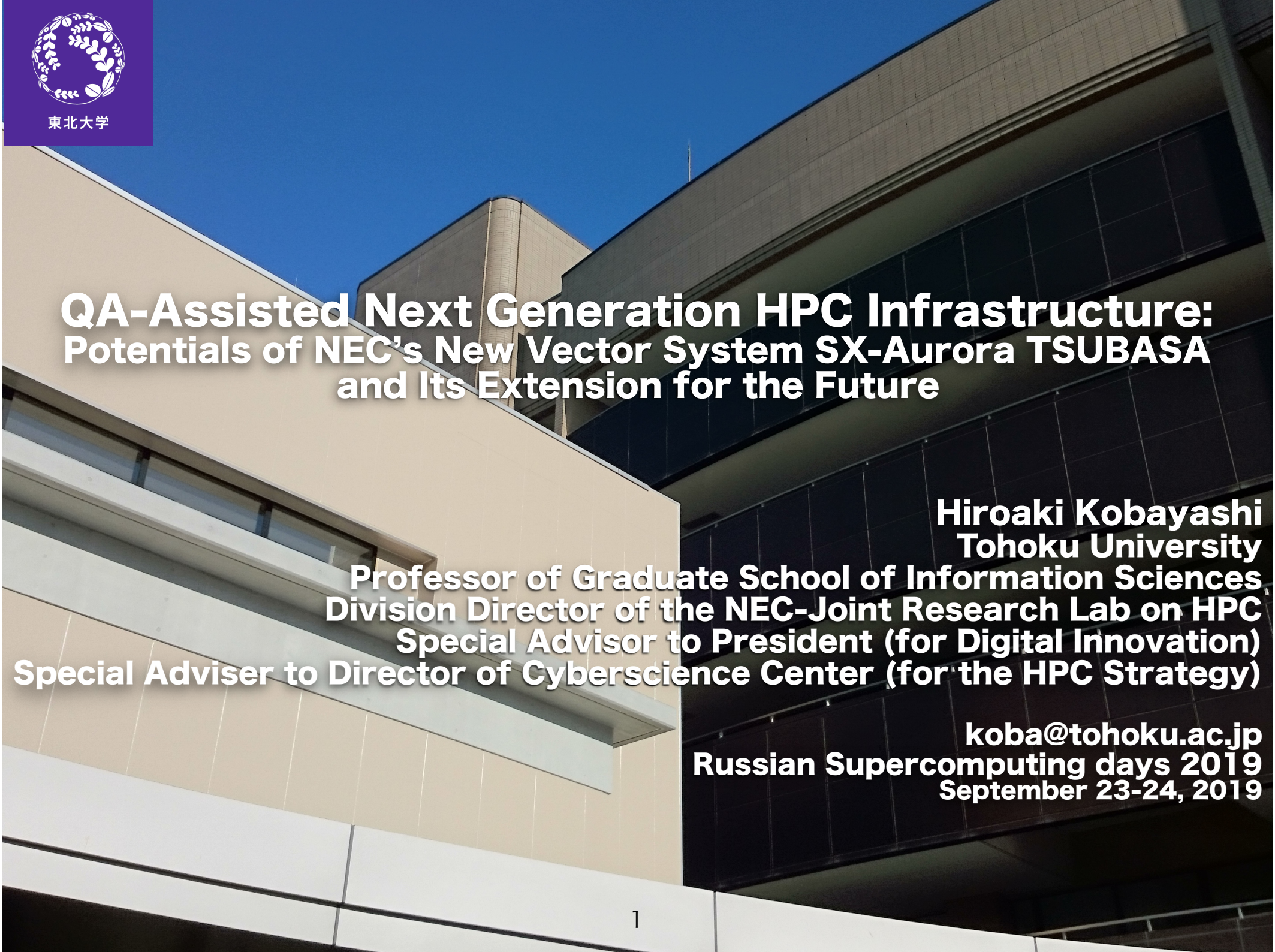

QA-Assisted Next Generation HPC Infrastructure:
Potentials of NEC's New Vector System SX-Aurora TSUBASA and Its Extension for the Future

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Professor of Graduate School of Information Sciences
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Special Adviser to Director of Cyberscience Center (for the HPC Strategy)

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Russian Supercomputing days 2019
September 23-24, 2019

Today's Agenda

- ★ Science and Technology Policy in Japan toward Society 5.0
- ★ R&D of a Quantum Annealing-Assisted HPC Infrastructure and its Killer Apps
  - New-Generation HPC Infrastructure based on Vector-Scalar and Quantum-Annealing Hybrid
  - New-Generation Applications based on Simulation-AI・ML Fusion
    - ✓ Tsunami inundation forecasting and evaluation planning
    - ✓ Digital Twin of Numerical Turbine for High-Performance Turbine Design and Dependable Operations
    - ✓ QA-assisted Material Informatics Infrastructure

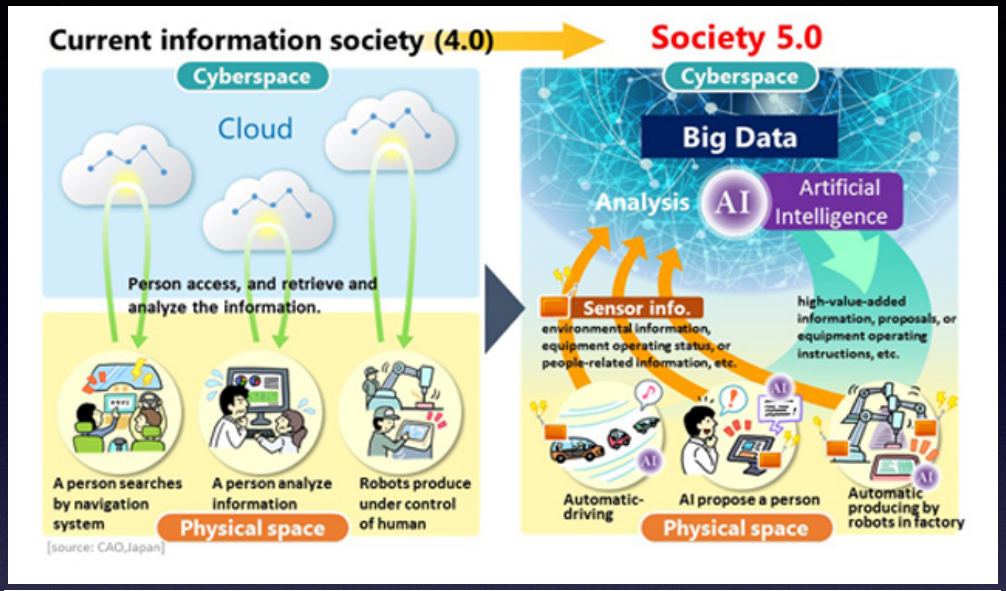
5th Science and Technology Basic Plan 2016-2020 in Japan
Promoting activities toward the actualization of Society 5.0

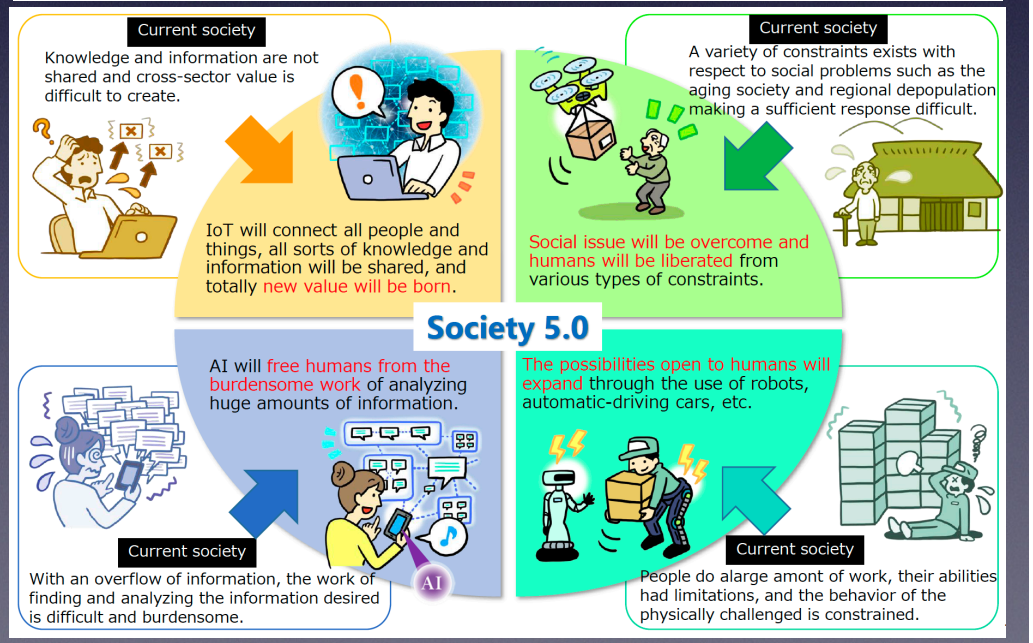
★ What is Society 5.0

- ✓ A human-centered society that balances economic advancement with the resolution of social problems by a system that highly integrates cyberspace and physical space.

★ Key Infrastructures and technologies to support the Society 5.0 world

- ✓ Cyber-Physical System, Close Interaction and convergence between Physical Space and Cyber Space, is a key infrastructure of Society 5.0
- ✓ A large amount of data in the physical space collected by using the IoT technology are now combined with simulation data in the cyberspace,
- ✓ AI, high performance data processing, exploits higher-order information from the cyber and physical data, and controls the cyber-systems and real-systems to maximize values, productivities, sustainability, safety… of any kinds of social activities, life, engineering, as well as advance of science.





Source: Cabinet office of Japan

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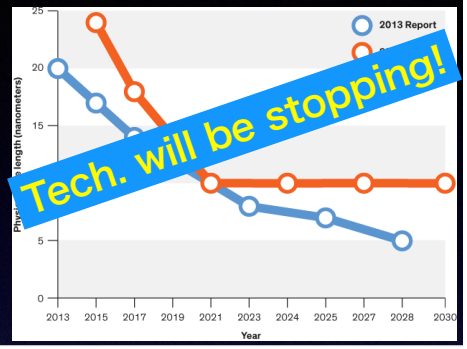
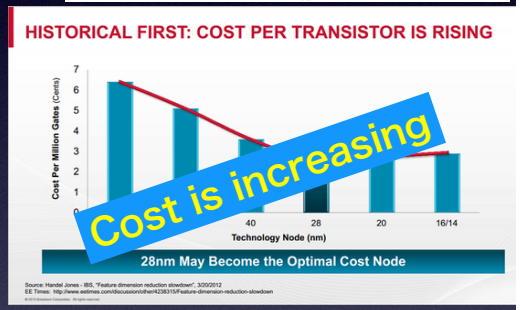
Yes, Scaling may be End, but Silicon is not End! And Use it Smart and Effective!



- ✓ We are facing the end of Moore's low due to the physical limitations, and the transistor cost is hard to reduce, however
- ✓ Tech. is slowing, cost is increasing, and efficiency is lowering!
- ★ Silicon is still fundamental constructing material for computing platforms such as plastic, steel and concrete for automobiles, buildings and home appliances.



So, we have to become much more smart for design of Future HEC systems.

Use precious silicon budget (+ advanced device technologies) to effectively design mechanisms that can maximize the sustained performance of individual applications.

Top 10 Systems on November 2018 TOP500 List

Rank	Name	Manufacturer	Country	Total Cores	Rmax [TFlops]	Rpeak [TFlops]	Rmax/ Rpeak
1	Summit	IBM	United States	2,397,824	143,500	200,795	71%
2	Sierra	IBM / NVIDIA / Mellanox	United States	1,572,480	94,640	125,712	75%
3	Sunway TaihuLight	NRCPC	China	10,649,600	93,015	125,436	74%
4	Tianhe-2A	NUDT	China	4,981,760	61,445	100,679	61%
5	Piz Daint	Cray Inc.	Switzerland	387,872	21,230	27,154	78%
6	Trinity	Cray Inc.	United States	979,072	20,159	41,461	49%
7	AI Bridging Cloud Infrastructure (ABCI)	Fujitsu	Japan	391,680	19,880	32,577	61%
8	SuperMUC-NG	Lenovo	Germany	305,856	19,477	26,874	72%
9	Titan	Cray Inc.	United States	560,640	17,590	27,113	65%
10	Sequoia	IBM	United States	1,572,864	17,173	20,133	85%

Rmax/ Rpeak
71%
75%
74%
61%
78%
49%
61%
72%
65%
85%

It's time to focus on Balanced Architectures for the wider-range of applications, and Domain-Specific Architectures for computation-intensive, memory-intensive, I/O intensive, low-precision computing… etc applications to improve silicon/power efficiency!

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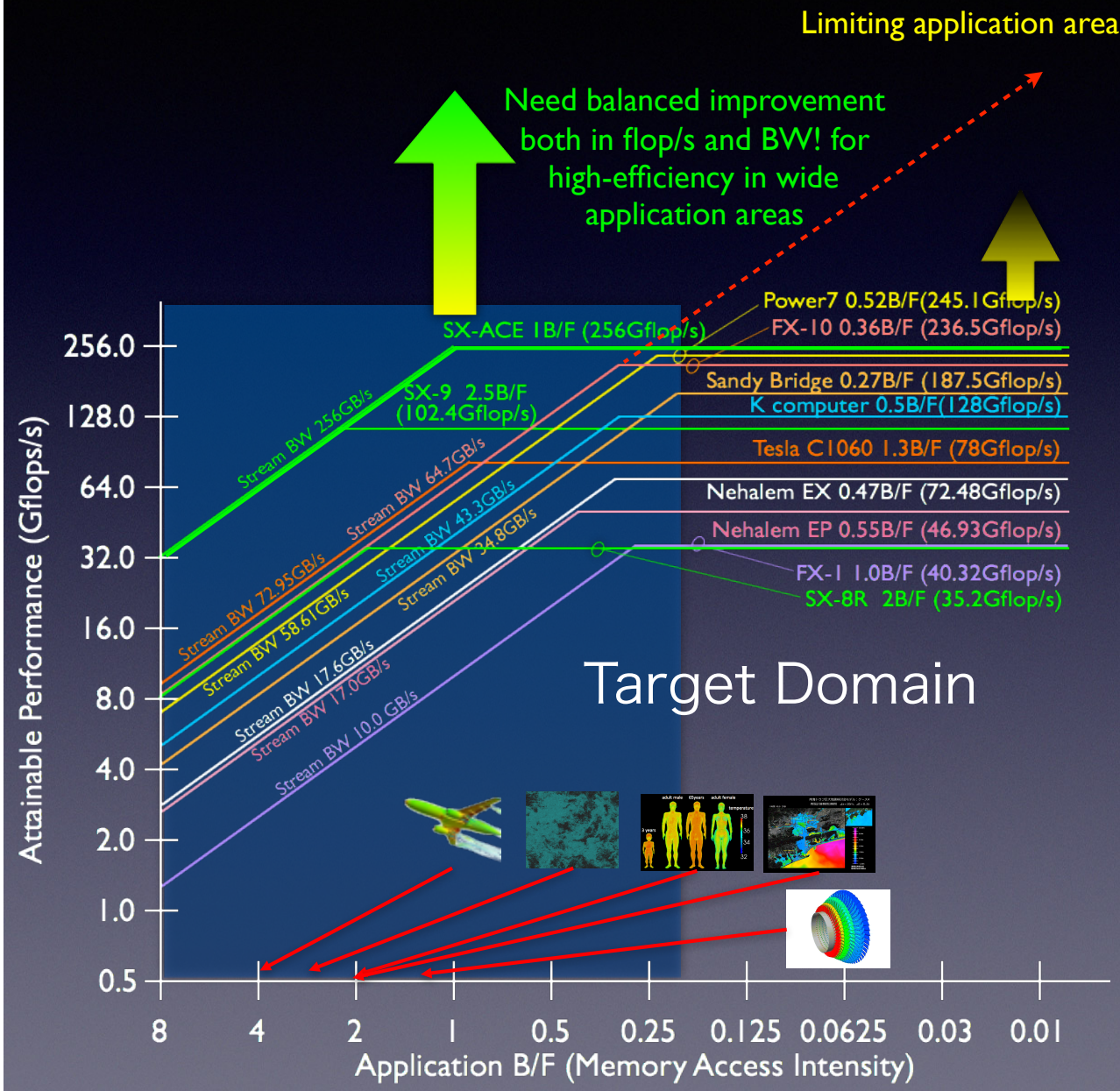
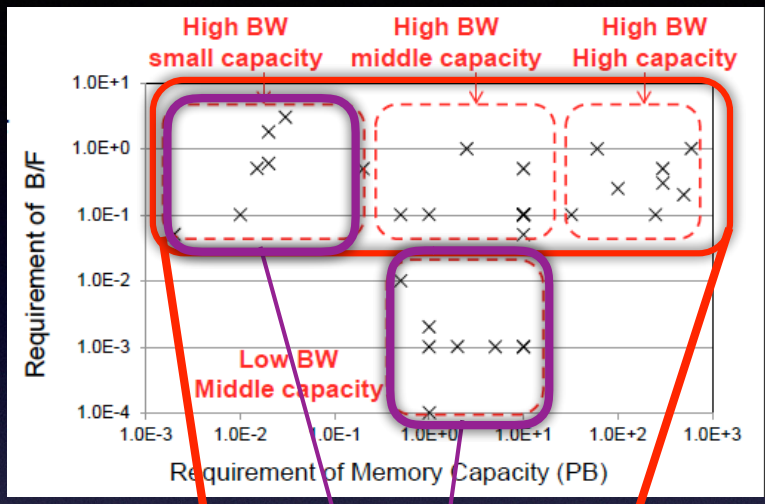
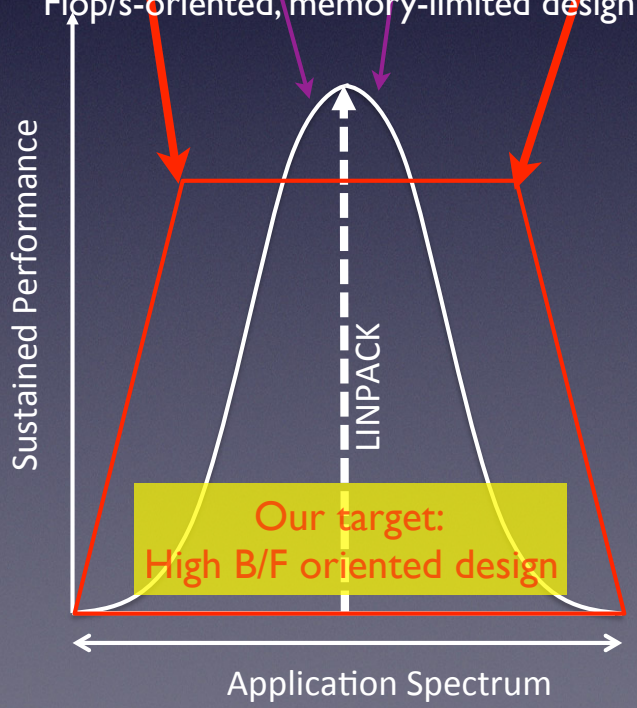
Our Approach of Balanced Architecture Design: Not Peak Performance, Turn Memory-BW into Sustained Performance!

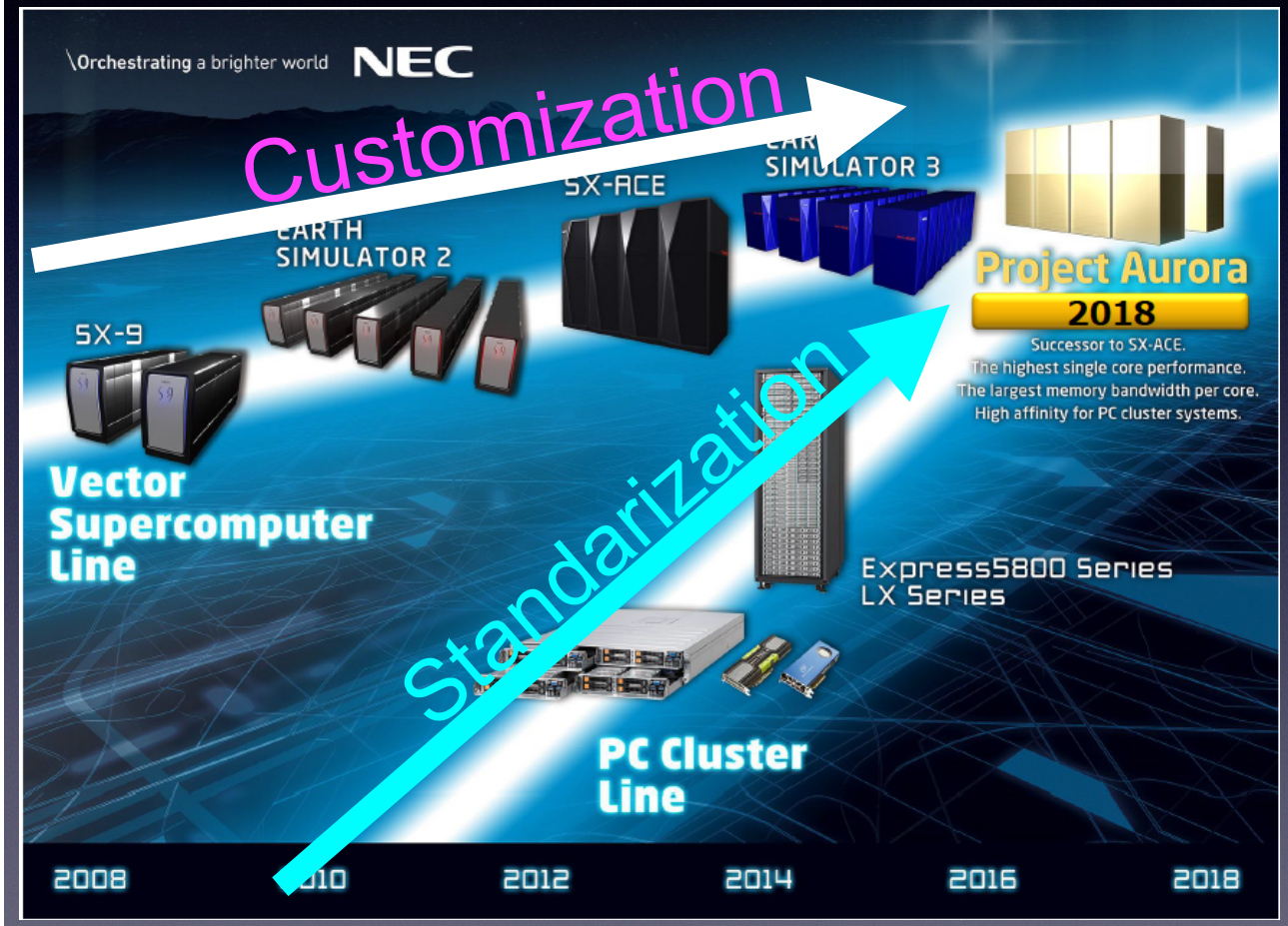




Flop/s-oriented, memory-limited design



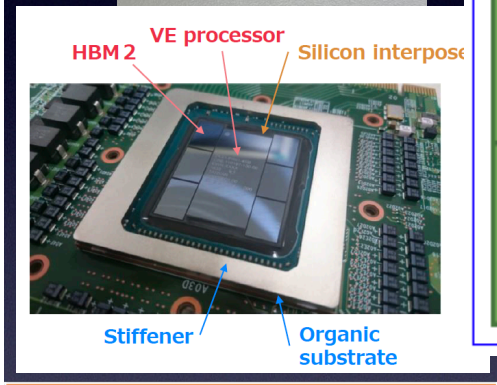
Why Vector System: SX-Aurora-TSUBASA?



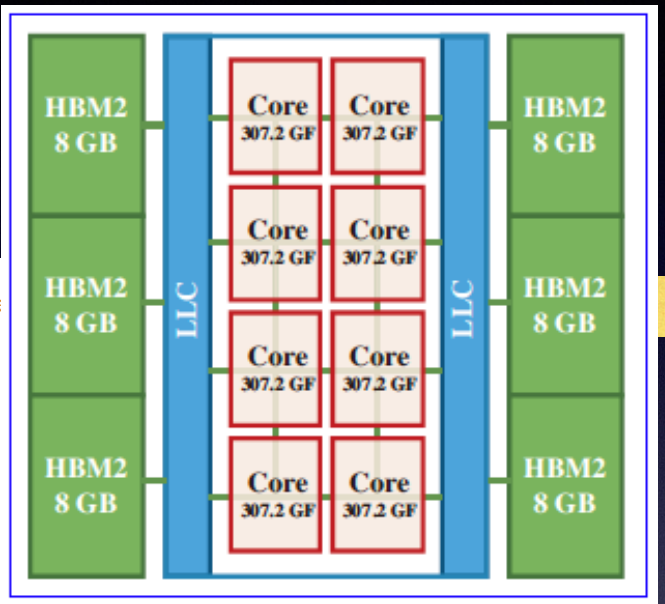
Source: NEC

- ★ Customization for realization of the balanced architecture
  - ✓ Highest Mem. BW
  - ✓ Largest Single Core Performance
- ★ Standardization for realization of the user-friendly environment
  - ✓ Linux Environment
  - ✓ New execution model centralized on vector computing

Hardware Specification of SX-Aurora TSUBASA

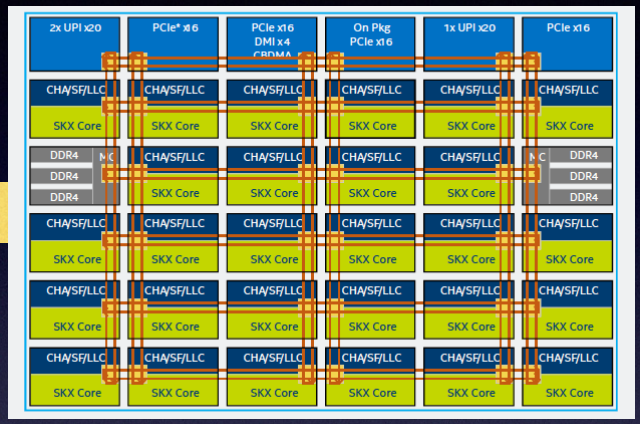


SX Vector Processor



PCIe

X86 Processor(Xeon)



Vector Engine (VE)	Type 10B
Frequency	1.4 GHz
Performance/Core	537.6 GF(SP), 268.8 GF (DP)
No. of Cores	8
Performance/Socket	4.30 TFLOPS (SP) 2.15 TFLOPS (DP)
Memory Subsystem	HBM2 8GB x6
Memory Bandwidth	1.2 TB/s
Memory Capacity	48 GB

Vector Host (VH)	Intel Xeon Gold 6126
Frequency	2.60 GHz / 3.70 GHz (Turbo boost)
Performance/Core	166/236 GF(SP), 83/118 GF (DP)
No. of Cores	12
Performance/Socket	1,996/2,840 GF(SP) 998.4/1,420 GF(DP)
Memory Subsystem	DDR4-2666 DIMM 16GB x 6
Memory Bandwidth	128 GB/s
Memory Capacity	96 GB

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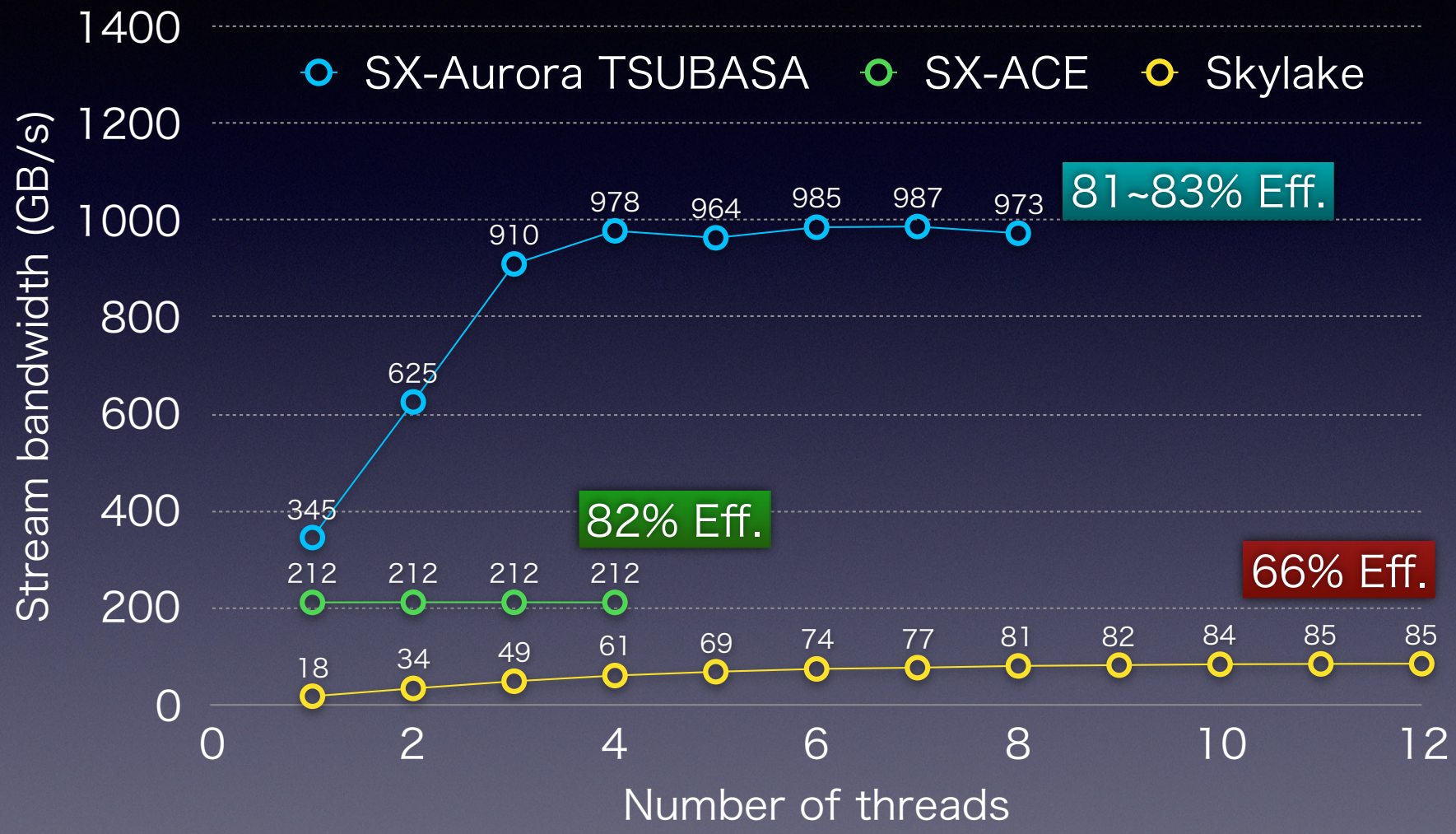
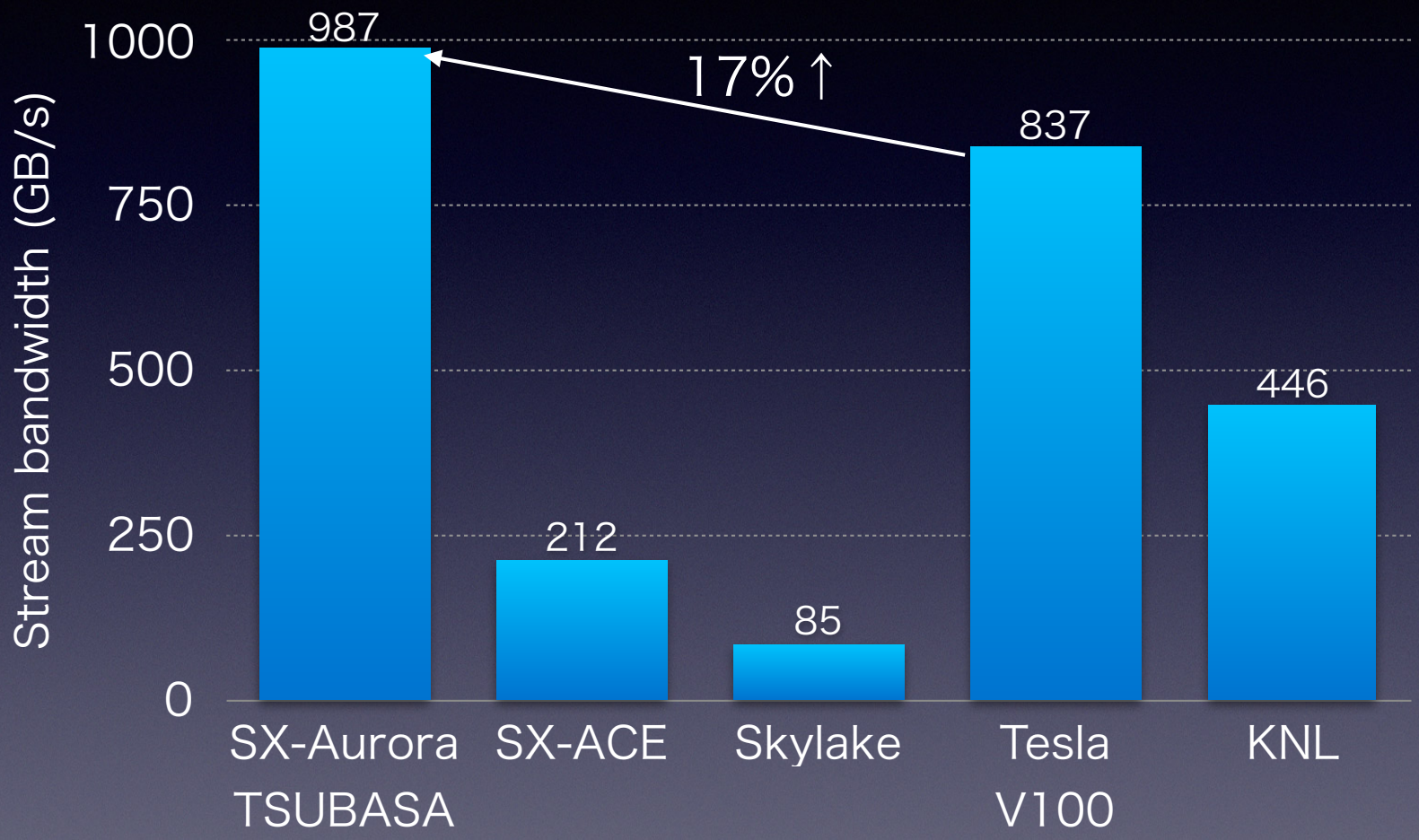
SX-Aurora TSUBASA is an Example of the Balanced Architecture

	Intel Xeon Gold 6126	NEC Vector Engine Type	NVIDIA Tesla V100	Intel Xeon Phi
Frequency	2.6 GHz / 3.7 GHz(Turbo)	1.4 GHz	1.245 GHz	1.5GHz
No. of cores	12	8	5120	72
Core Performance	166/237 GF (SP) 83.2/118 GF (DP)	538GF (SP) 269GF (DP)	2.73GF (SP) 1.37GF (DP)	96GF (SP) 48GF (DP)
Performance/ socket	2.0/2.8 TF (SP) 1.0/1.4 TF (DP)	4.3 TF (SP) 2.15 TF (DP)	14 TF (SP) 7 TF (DP)	6.9 TF (SP) 3.5 TF (DP)
Memory subsystem	DDR4-2666 DIMM 16GB x 6	HBM2 8GB x 6 modules	HBM2 4GB x 4 modules	MCDRAM+ DDR4-2400
Memory bandwidth	128 GB/s	1.22 TB/s	900 GB/s	450GB/s (MCDRAM) 115.2GB/s(DDR)
Memory capacity	96 GB	48 GB	16 GB	16GB(MCDRAM) 96GB(DDR)
B/F	0.13	0.57	0.13	0.13

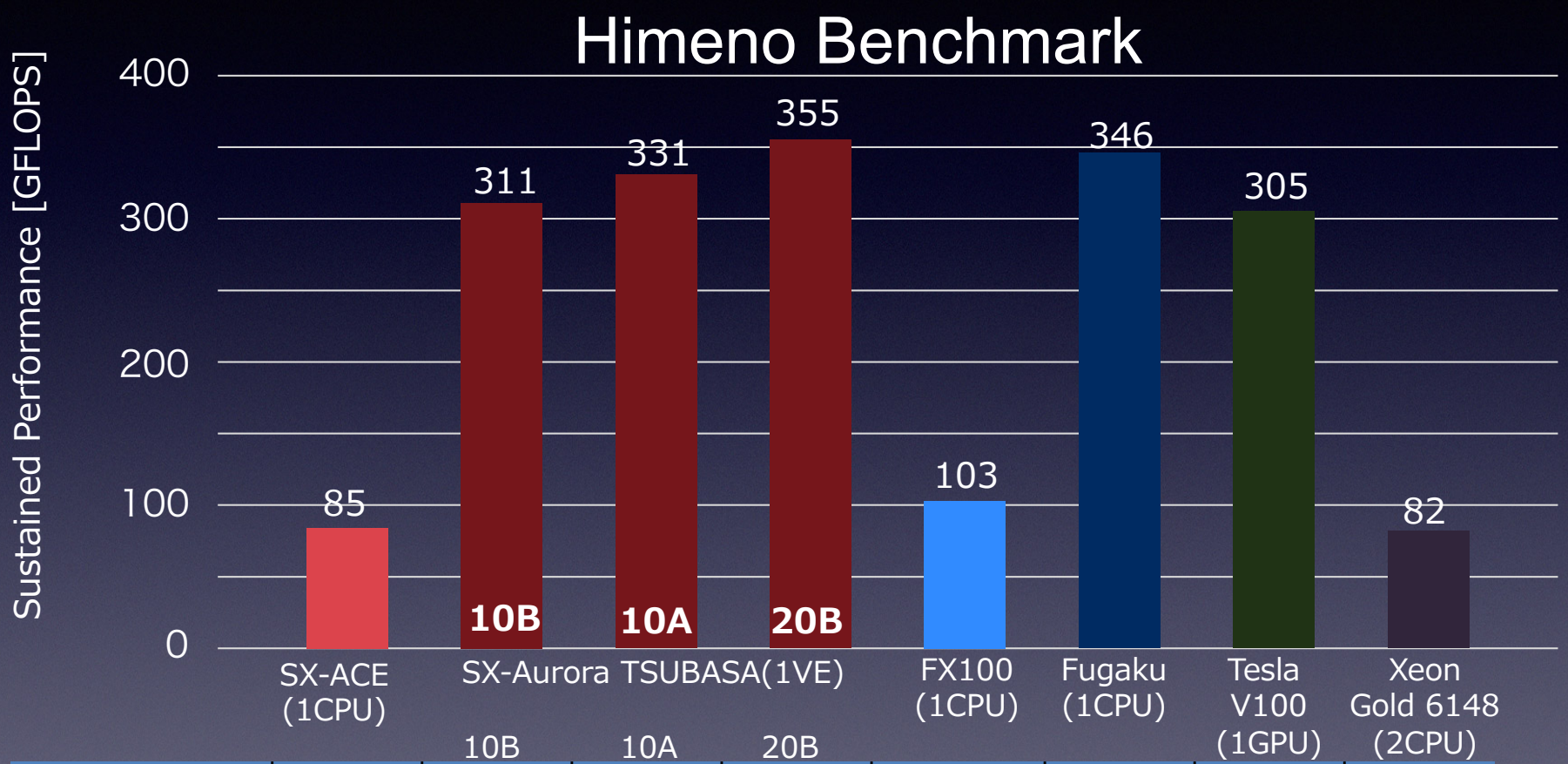
STREAM Benchmark Results: Sustained Memory Throughput



STREAM Benchmark Results: Socket Performance

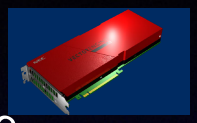


The Memory Performance: The dominant factor for a high-sustained performance



		10B	10A	20B				
Peak(DP)[TF]	0.256	2.15	2.45	2.45	1.12	2.7	7	3.07
MemBW[TB/s]	0.256	1.22	1.22	1.53	R:0.240 W:0.240	1.024	0.90	0.256

What Does the Next Vector System Look Like in Year Around 2021-2022?



Aurora in 2018

New Generation Aurora in 2022?

■New Developed Vector Processor
■PCIe Card Implementation, but not an accelerator
■8 cores / processor
■2.45TF performance
■1.2TB/s memory bandwidth
■Normal programing with Fortran/C/C++

★Vector Engine Spec.

- The 7nm Technology becomes available?
  - 5X more transistors from 16nm tech?
  - 5X in # of Cores, i.e. 50 VE cores feasible?
  - up to 15TF, if the core performance is same, but should be lowered due to power/thermal limitation of the chip.

★Memory Subsystem

- 2x in Memory BW, and 1.5X in Memory Capacity when using HBM 3 under the assumption of the same chip size of Aurora-TSUBASA
  - ~3TB/s and ~96GB??

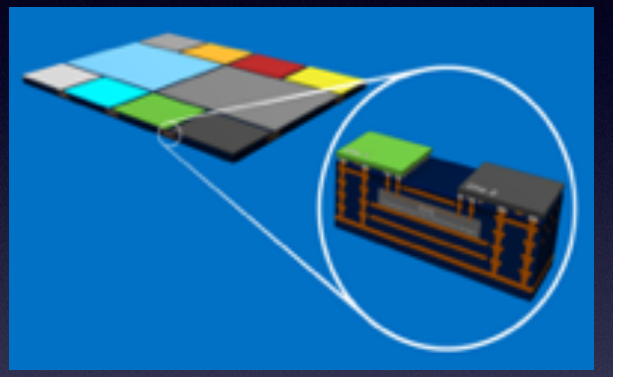
★Design space exploration of 0.5BF (20 cores of 6TF for memory-intensive applications) to 0.25 BF (40 Cores of 12TF for compute-intensive applications)

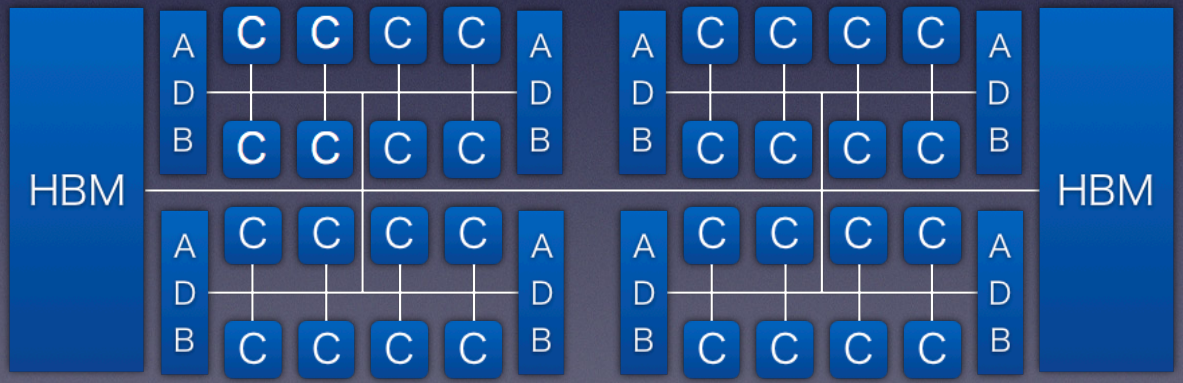
- be competitive with contemporary HEC systems at that time, such as Post-K (JP), A21 (US), NERSC-9 (USA), Crossroads (US), EU Exa-System (FR/GE), NUDT2020 (Ch)…

What Does the Next Vector System Look Like in Year Around 2021-2022? (Cont'd)

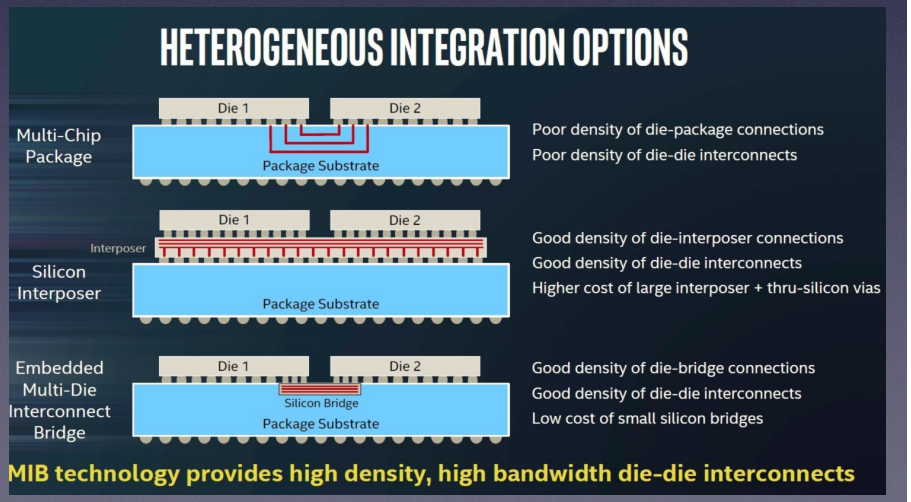
★How 20~40 cores are integrated, connected and organized.

- Single chip or multi-chip (SIP) ?
- If SIP is employed, how multiple chips are connected?
  - ✓If EMIB available, BW could be increased?
  - ✓Silicon photonics with WDM
- Single SMP or clustered SMP
- crossbar, mesh, ring, etc or their hierarchical and hybrid?
- coherency protocol of ADB (Snoopy or Directory)



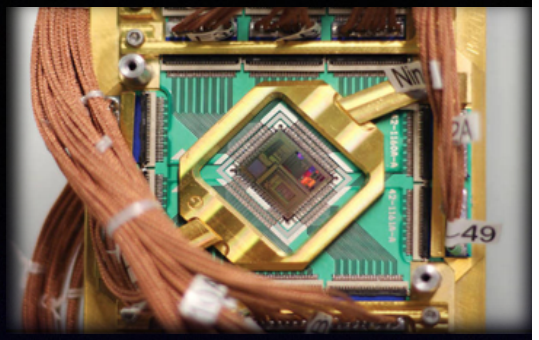


32 Cores, 9.6TF, 3TB/s, 0.3BF



Source by Intel

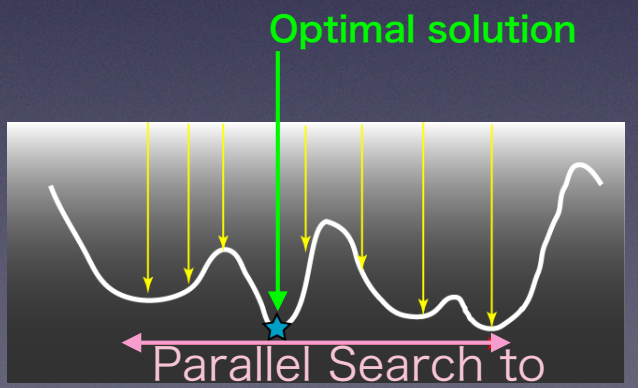
Quantum Computer: Emerging Domain Specific Architecture



- ★ Quantum computing is drawing much attention recently as an emerging technology in the era of post-Moore
  - ✓ In particular, quantum computers for quantum annealing are commercialized by the D-wave systems, and their applications are developed world-widely.
    - ✓ Google, NASA, Volkswagen, Lockheed, Denso…
  - ✓ The base model named the Ising model to design and implement the D-wave machines has been proposed by Prof. Nishimori et al of Tokyo Inst. Tech. In 1998.
- ★ The quantum annealing is a metaheuristic for finding the global minimum of a given objective function over a given set of candidate solutions (candidate states), by a process using quantum fluctuations

Source by D-Wave Sys.

Transverse magnetic field type quantum annealing Chip and System (D-Wave)



An ideal solver for combinatorial problems!

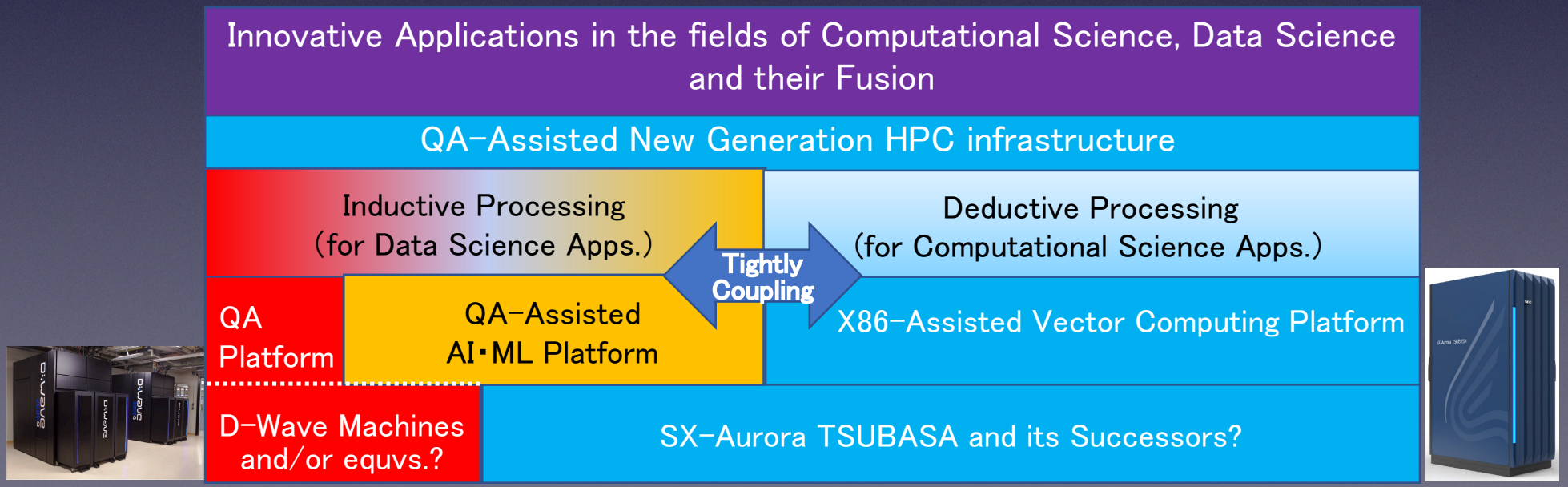
Toward Realization of Quantum Computing-Assisted HPC Infrastructure

★ Tohoku University has established an interdisciplinary priority research institute, named Q-HPC, for Quantum Computing-Accelerated HPC in 2018

★ As Q-HPC members, we start a new 5-year research program named "R&D of Quantum Annealing-Assisted HPC Infrastructure", supported by MEXT

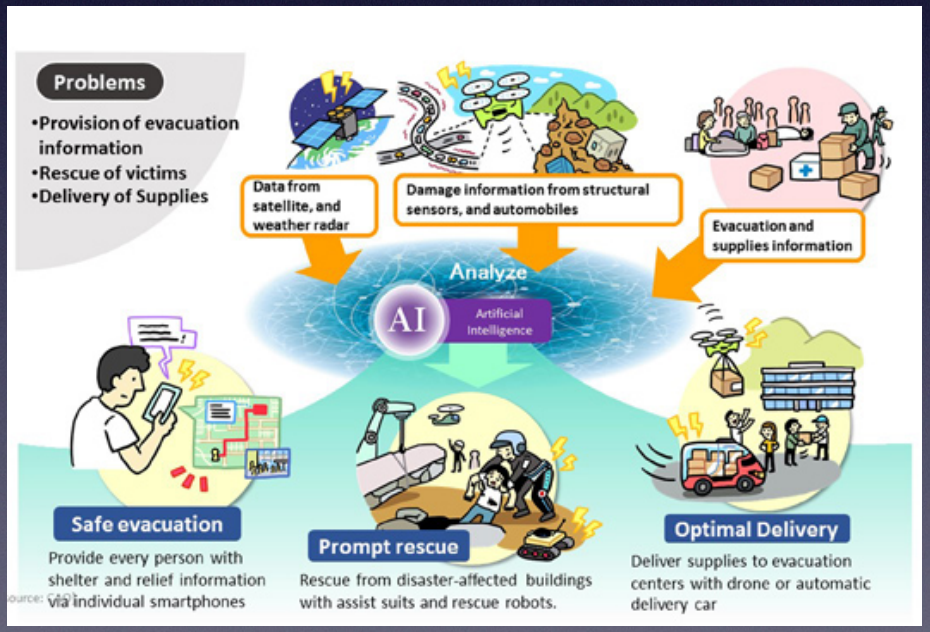
✓ Becomes an innovative infrastructure to develop next-generation applications in the fields of computational science, data sciences and their fusions

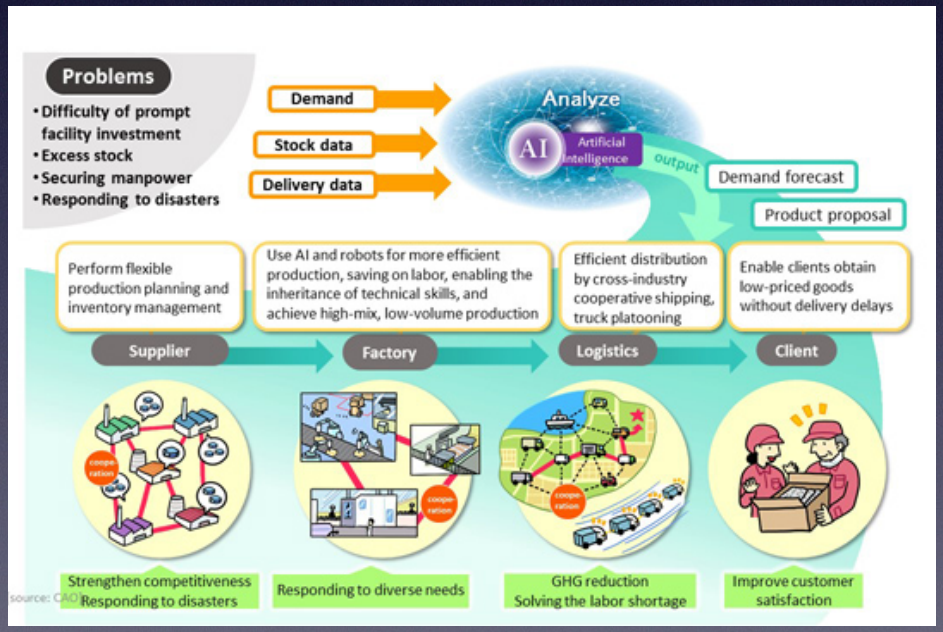
✓ provides transparent accesses to not only classical HPC resources but also Quantum Computing one in a unified fashion.



R&D of Next Generation Applications to Realize Society 5.0

- ★ Resilient Society against Natural Disasters
- ★ Efficient and Effective Maintenance of Social Infrastructures
- ★ Innovative and Productive Engineering
  - ✓Integrated Material Design and Development





Source: Cabinet office of Japan

Team Organization

★ PI: Hiroaki Kobayashi

Architecture/System Software Gr

Application Gr

AI・Machine Learning Gr

Quantum Annealing Gr

Digital Twin Numerical Turbine
Satoru Yamamoto, Osamu Watanabe et al. (Tohoku Univ).

Material Informatics
Tomonaga Okabe, Gota Kikugawa et al. (Tohoku Univ).

Real-Time Tsunami Inundation Damage Analysis and Optimal Evacuation Planning
Shun-ichi Koshimura et al (Tohoku Univ)

System Software:: Hiroyuki Takizawa, Ryusuke Egawa et al. (Tohoku Univ)
Akihiro Musa Yasuhisa Masaoka et al (NEC)

Inductive Processing

Tightly Coupling

Deductive Processing

Prof. Kazuhiko Komatsu (Tohoku Univ)
Takashi Hagiwara et al (NEC)

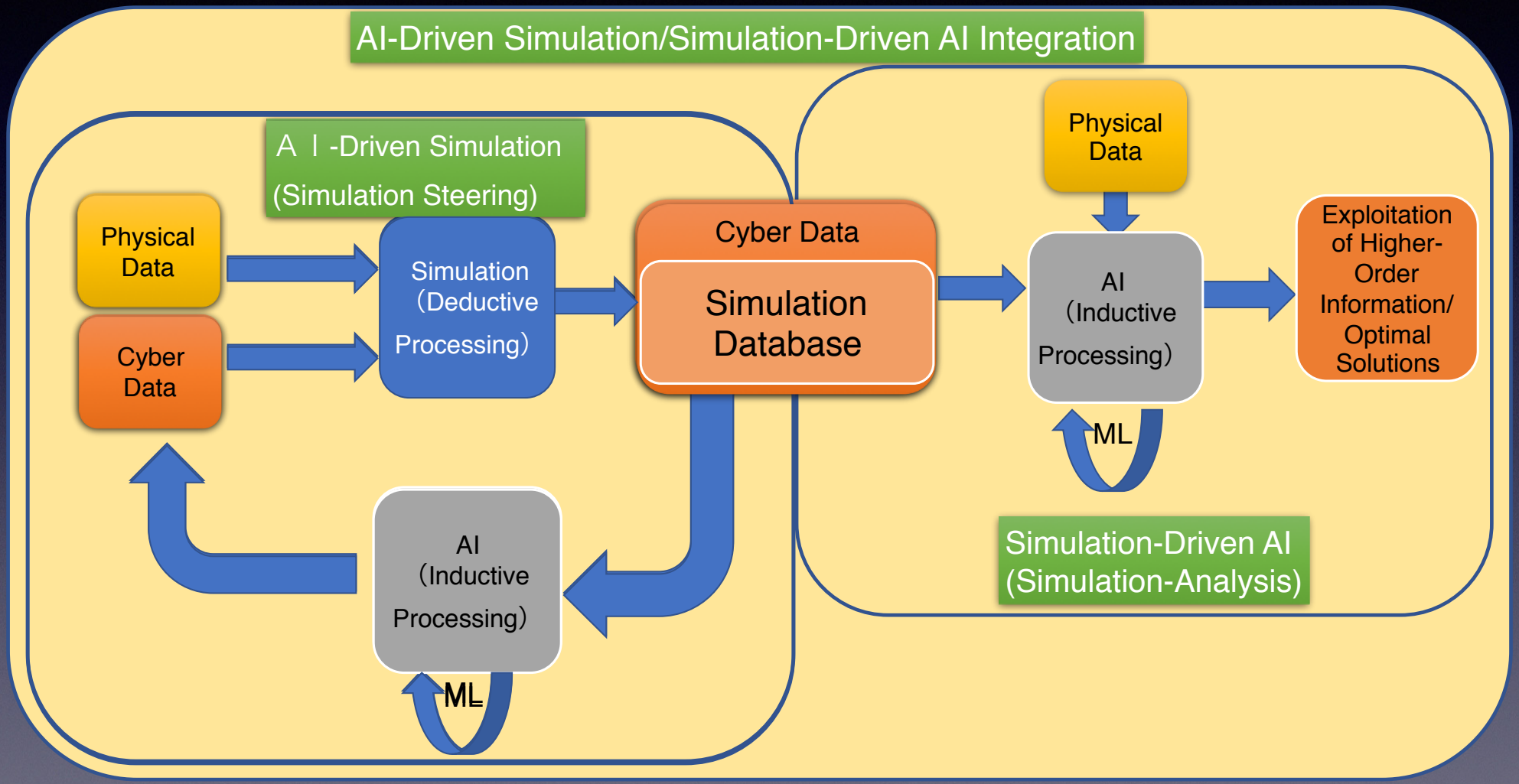
Architecture
Hiroaki Kobayashi et al (Tohoku Univ)
Mitsuo Yokokawa (Kobe Univ)

Masayuki Ozeki et al (Tohoku Univ)

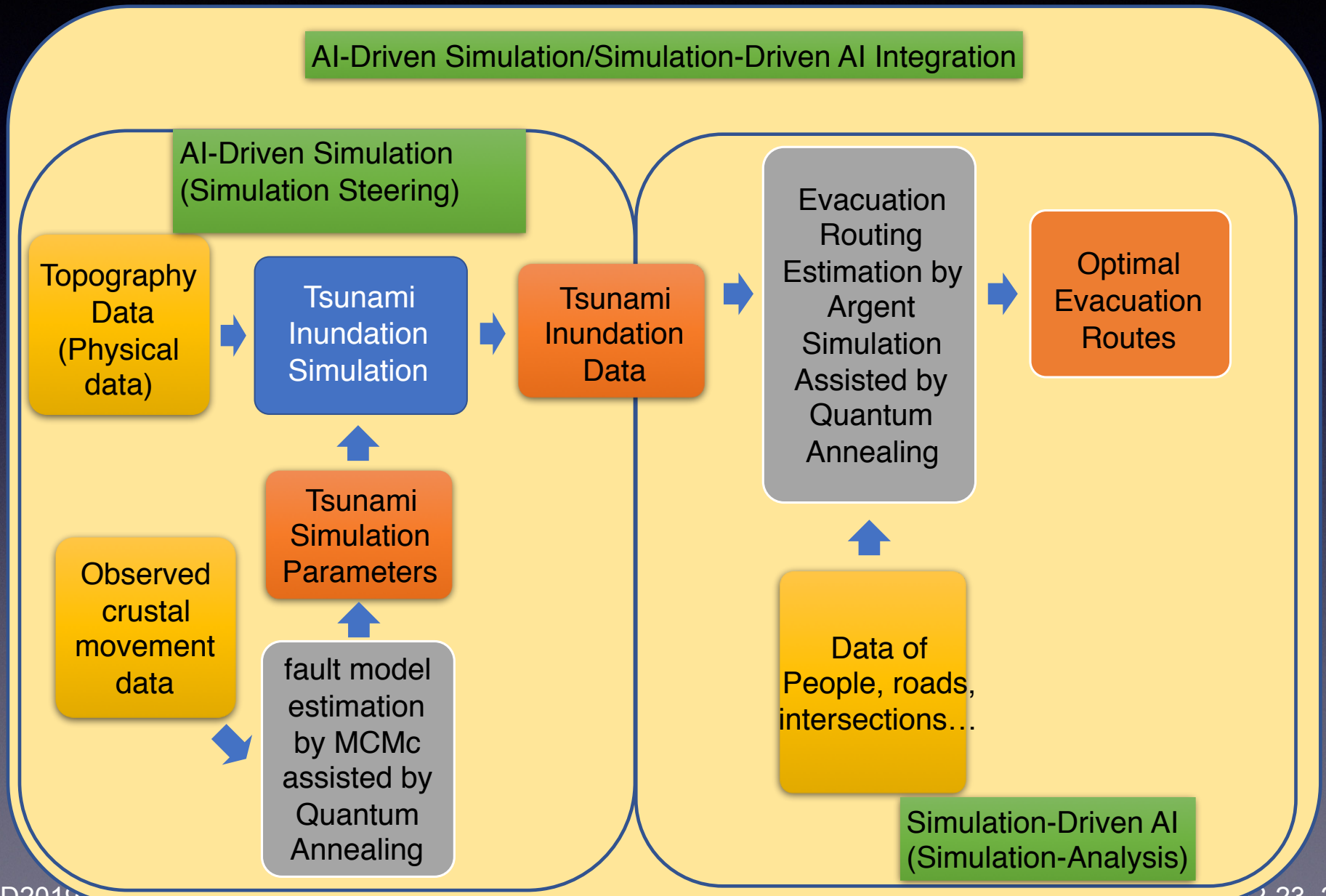
Shigeyuki Aino Shintaro Momose Yoko Isobe et al (NEC)

International Advisory Committee:
Mateo Valero (BSC,ES) Michael Resch (HLRS,DE), Vladmir Voevodin (MSU,RU),
Bo Ewald(D-wave, CA), Hans Peter Graf(NEC Lab. America, US)

Workflow Design of AI-Driven Simulation, Simulation-Driven AI and their Integration

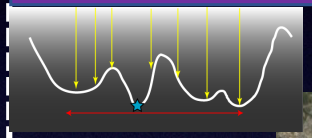


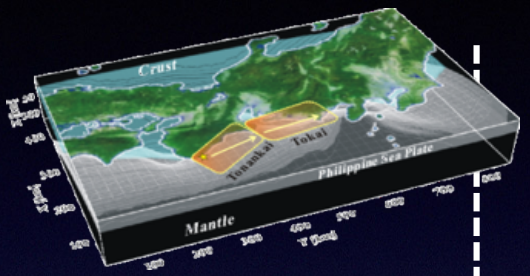
Workflow Design of Tsunami Inundation Damage Estimation and Optimal Evacuation Planning



Target Application 1: QA-Enhanced Real-Time Tsunami Inundation Forecasting and Optimal Evacuation Planning

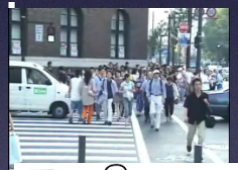
Fault Estimation with QA-enhanced MCMC





Tsunami Inundation Simulation

Optimal Evacuation Planning with Quantum Annealing



Integrated Programming Framework

D-wave Machine

Aurora TSUBASA Vector Host (Xeon)

Aurora TSUBASA Vector Engine

Tohoku University -Break limit of your potential- Quantum Annealing Research & Development
QARD
Supported by JST project for creating START

D-Wave The Quantum Computing Company™

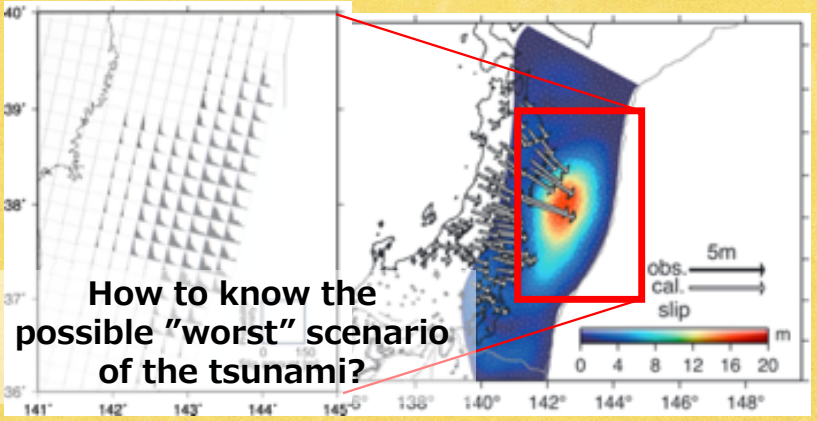
Empowered by Innovation NEC

Cyberscience Center

GSIS Graduate School of Information Sciences Tohoku University

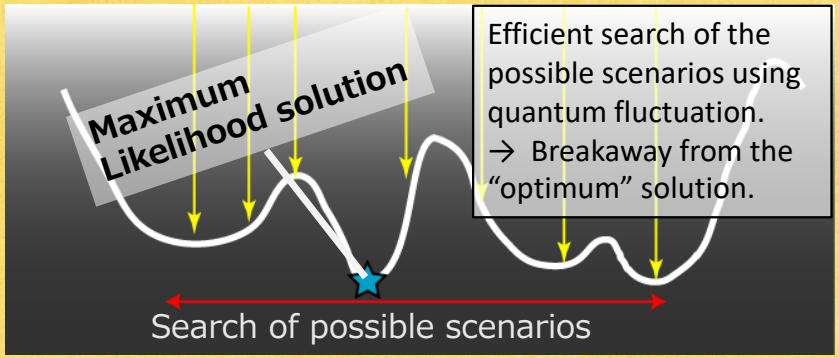
Quantitative Uncertainty Estimation of the Coseismic Fault Model using Quantum Fluctuation

●Difficulty of uncertainty estimation



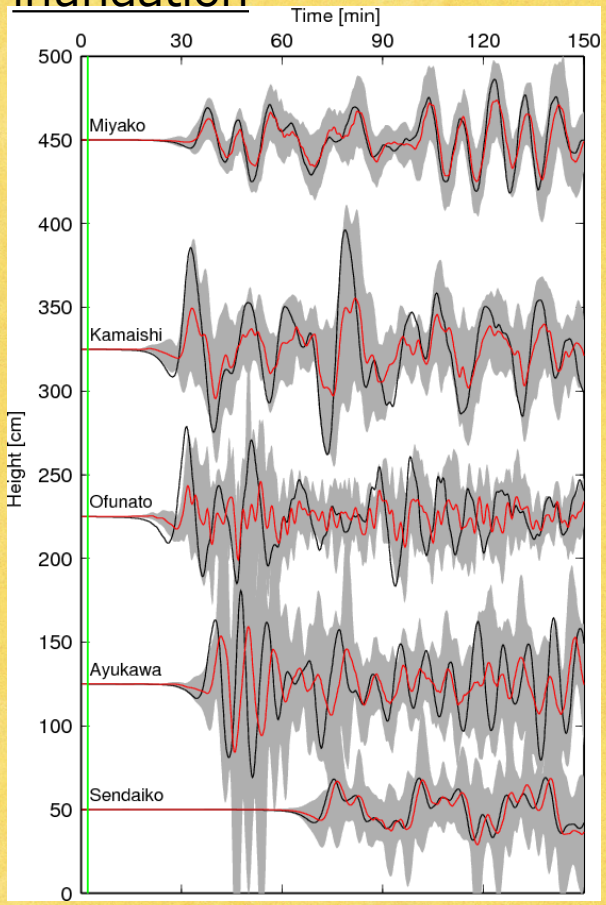
Rapid estimation by next Gen. vector computer

●Search and Assess. of ML solution



Utilizing excellent sampling ability of quantum computer

●Quantitative uncertainty estimation fo Tsunmi inundation

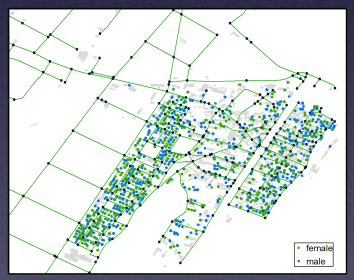


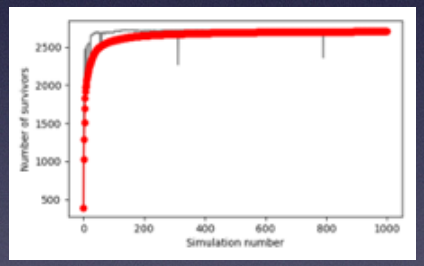
Hiroaki Kobayashi, Tohoku University

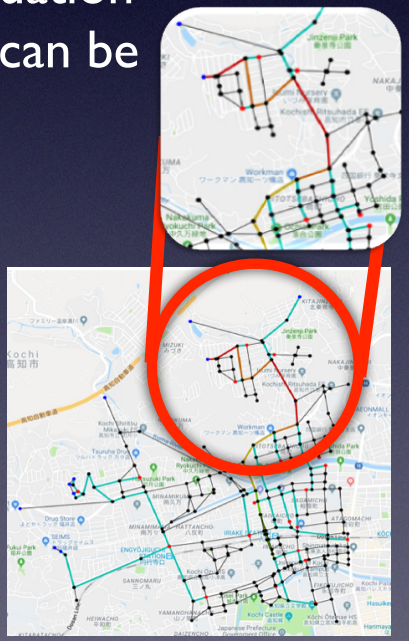
Real-Time Evacuation Guidance based on Multi-Agent Simulation, Reinforcement Learning and Quantum Annealing

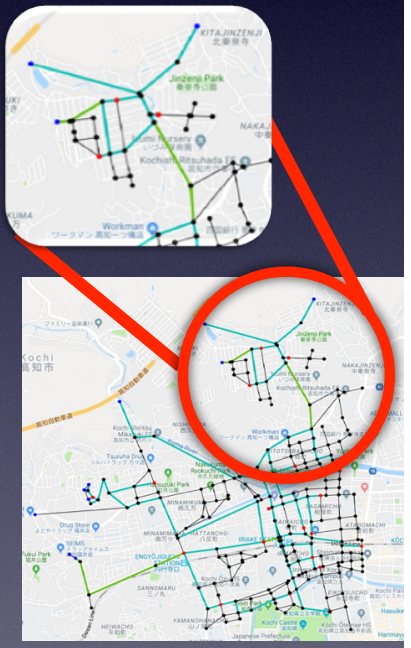
★ After tsunami inundation and building damage are estimated the best option for evacuation to safety zones is evaluated.

- ✓ Reinforcement Learning is used to evaluate multiple scenarios of evacuation and obtain optimal (fast evacuation, less casualty, less congestion) scenarios for the study area.
- ✓ Quantum annealing is used to optimize the evacuation decision so that congestion and safe evacuation can be accomplished.









Conventional QA-Optimized

Evacuation Flow Control

Integrated Programming Framework

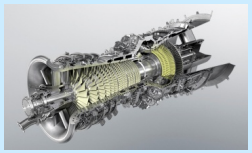
D-wave Machine

Aurora TSUBASA Vector Host (Xeon)

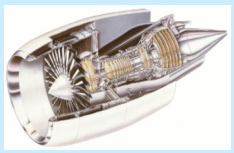
Aurora TSUBASA Vector Engine

Numerical Turbine: High Performance Turbine Design Code on SX Systems

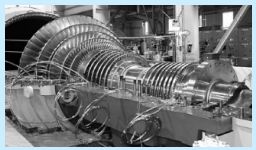
Numerical Turbine developed by Prof. Yamamoto of Tohoku University
- is a simulation code realizing High-performance and High-reliable Future Turbines and
- has been accelerated on the SX series of Cyberscience Center at Tohoku University.



Gas turbine for plants

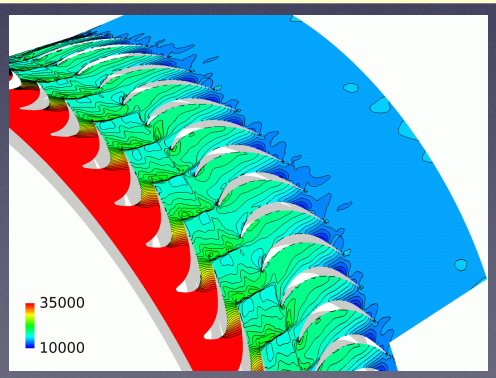


Gas turbine for airplanes

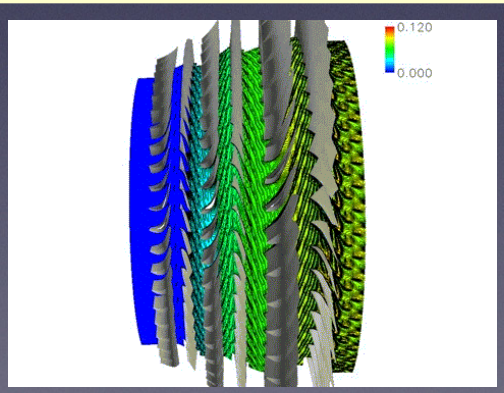


Steam turbine

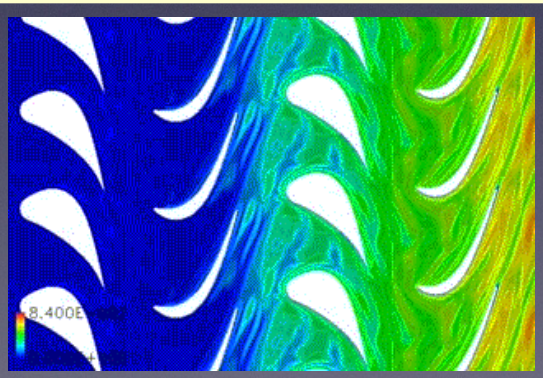
- Unsteady flows with wetness and shocks dominate actual gas turbines and steam turbines → Resolving such complex flows is crucial for developing high-performance and high-reliable turbines
- Full annulus (maru-goto) simulation is quite attractive and powerful for resolving unsteady wet-steam and moist-air flows in actual turbines and compressors
- Only Numerical Turbine has achieved such simulations in the world.



Unsteady shocks generated in turbine stage



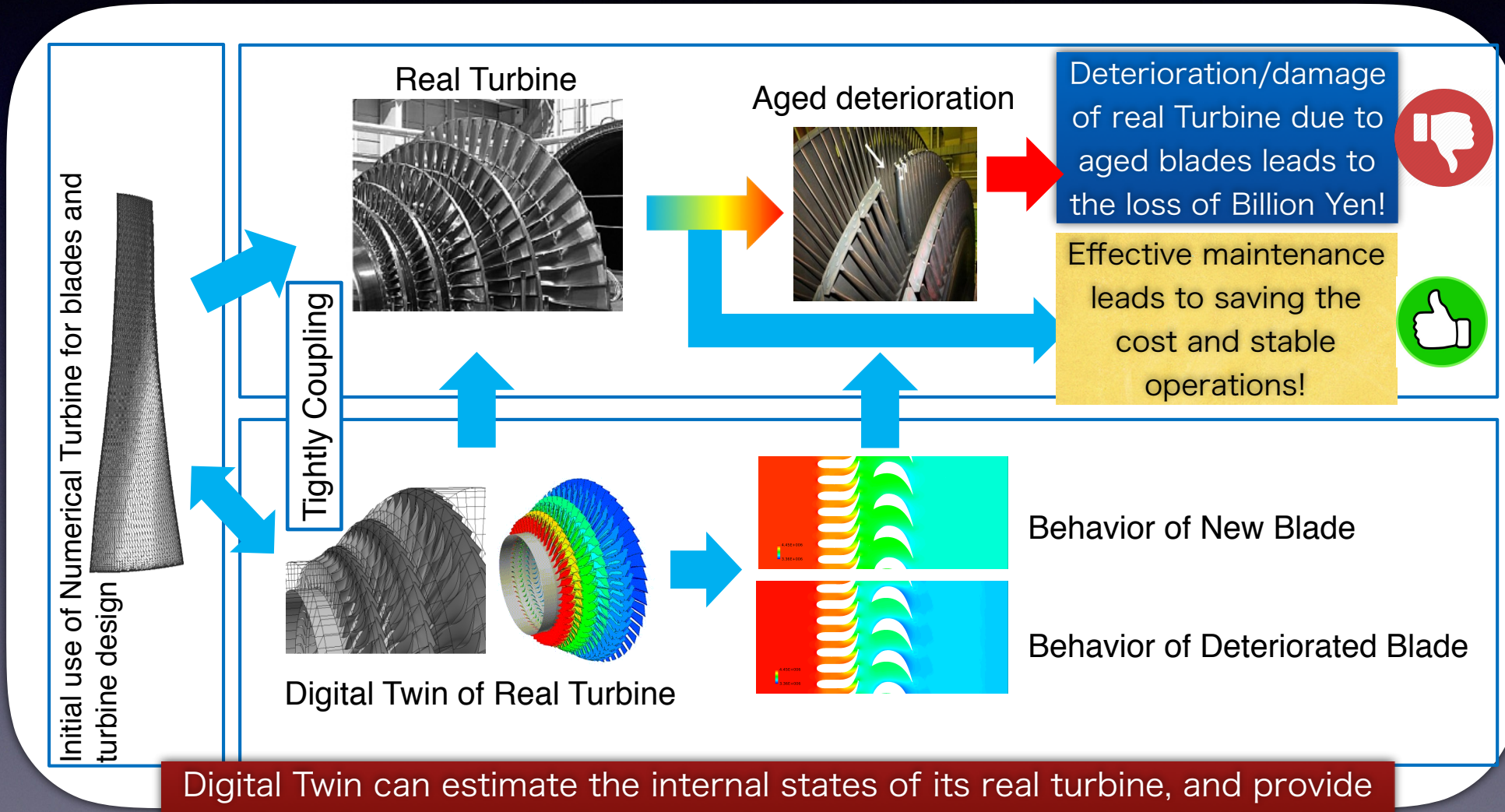
Unsteady wetness in full annulus turbine stages



Unsteady wet-steam flow in turbine stages

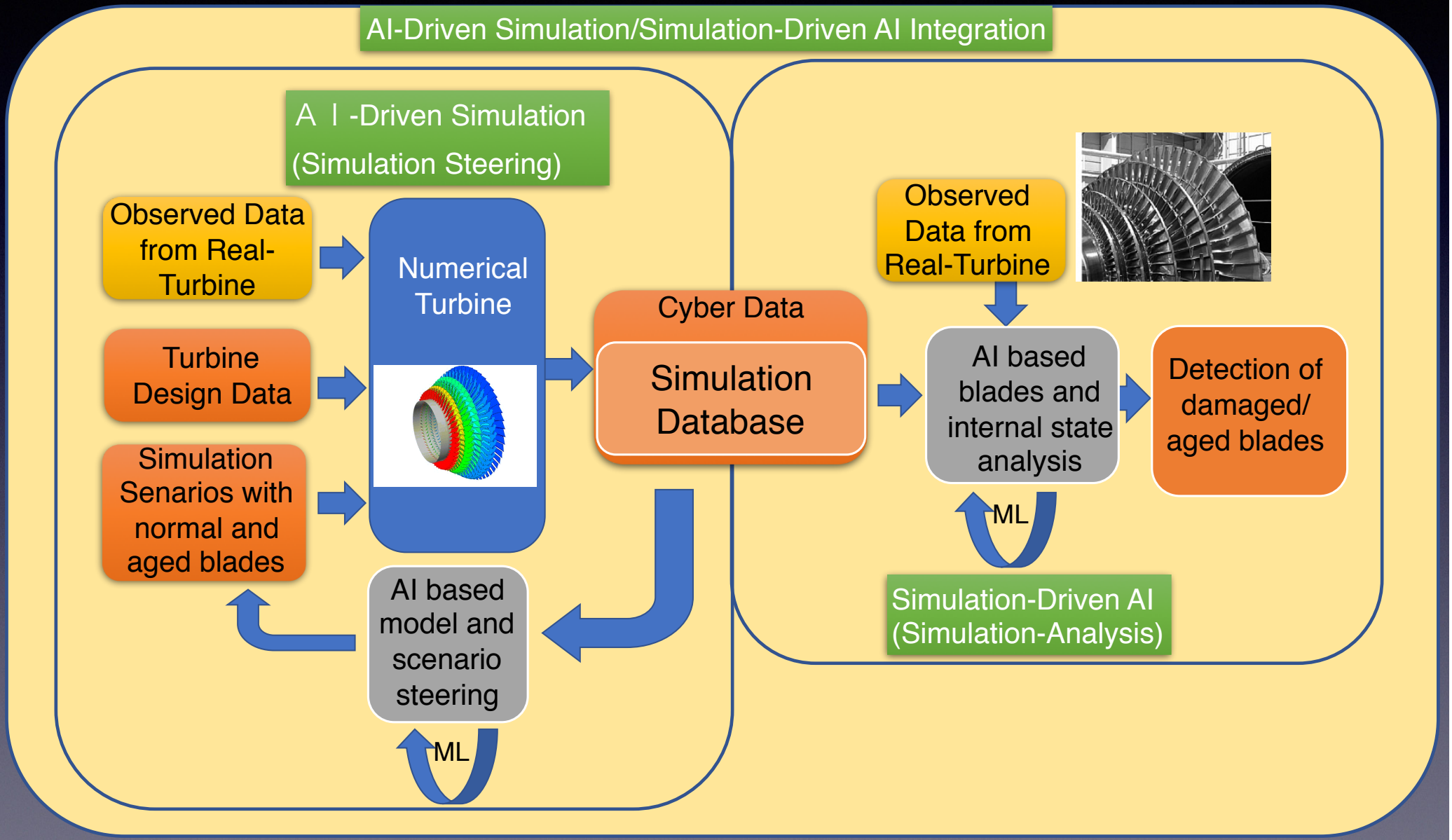
Realization of Digital Twin of Real-Turbine by Numerical Turbine

By examining the behavior of digital twin, appropriate maintenance and malfunction detection of its real turbine could be possible!

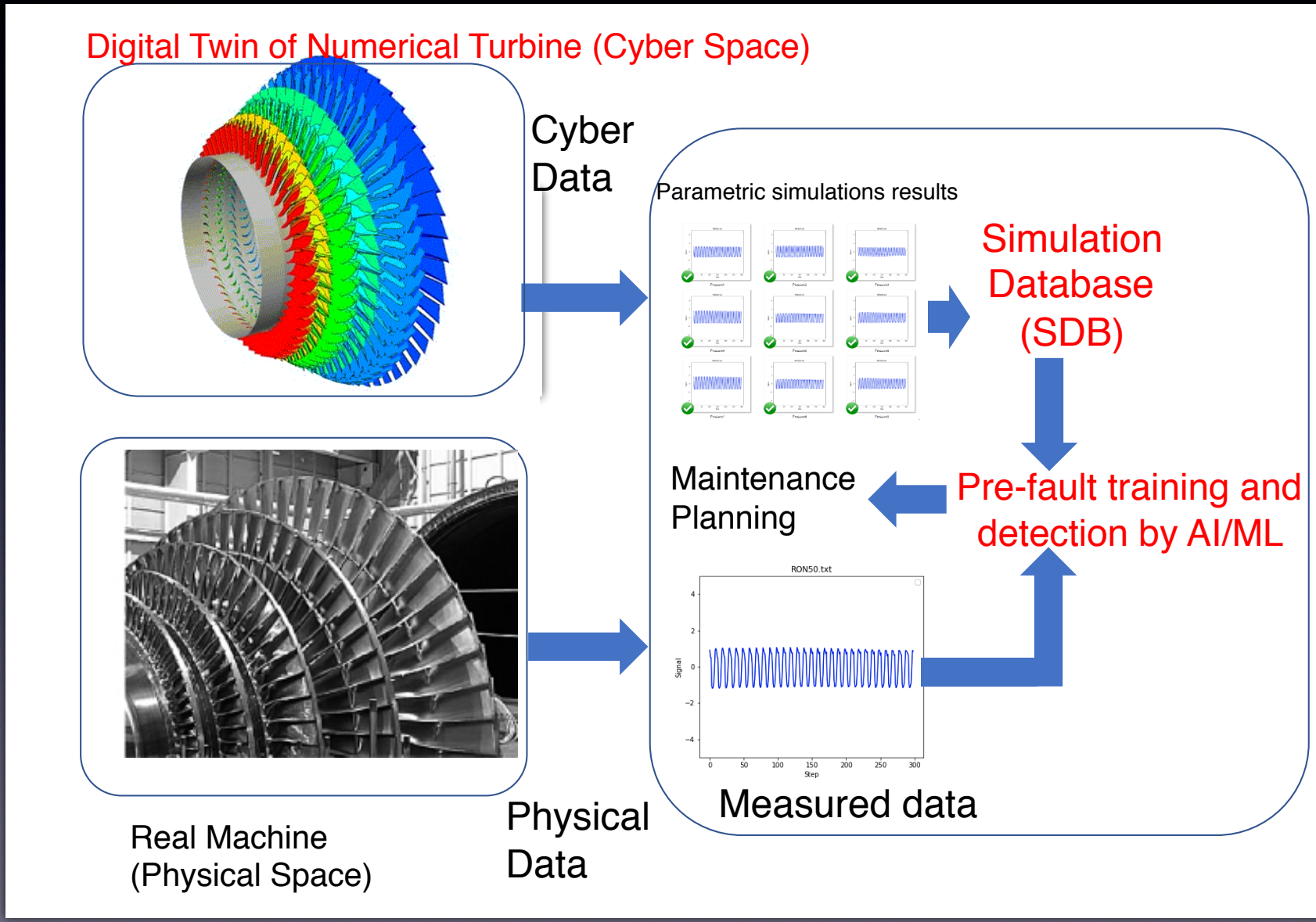


Digital Twin can estimate the internal states of its real turbine, and provide the information of effective maintenance to avoid serious incident!

Workflow of Digital Twin Application

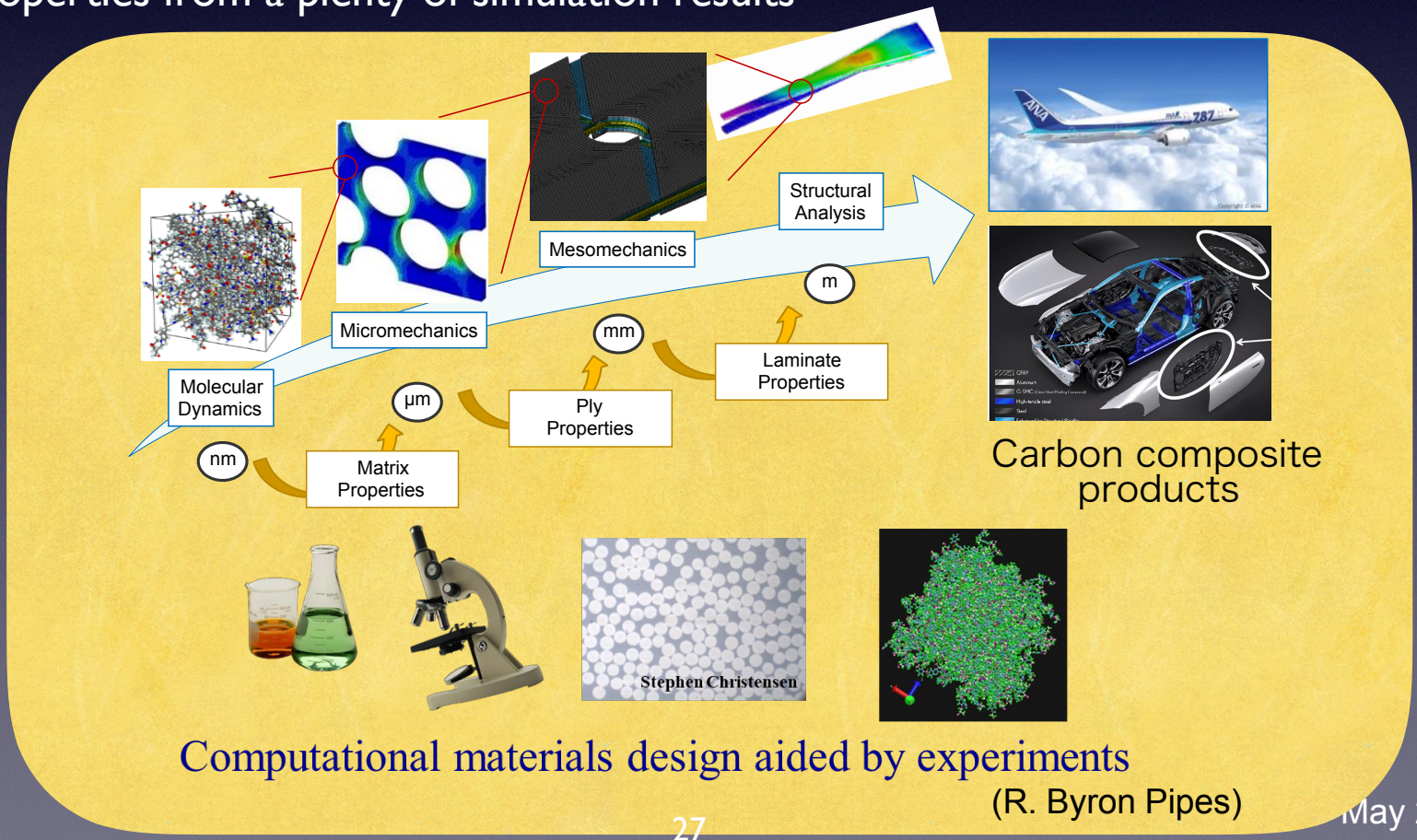


An Example of Target Applications: Digital Twin Numerical Turbine

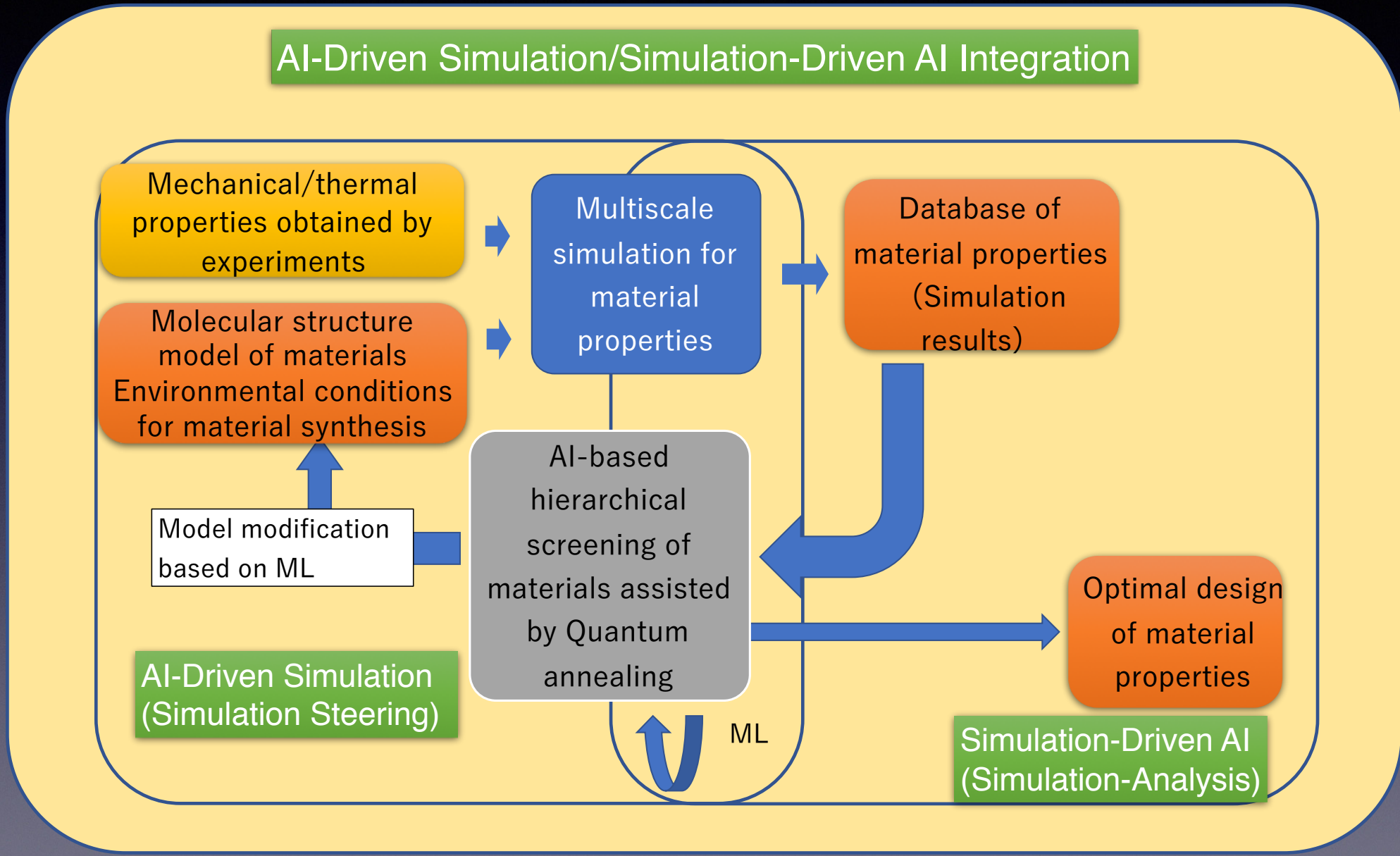


Target App. 3: QA-Assisted Materials Informatics Infrastructure R&D

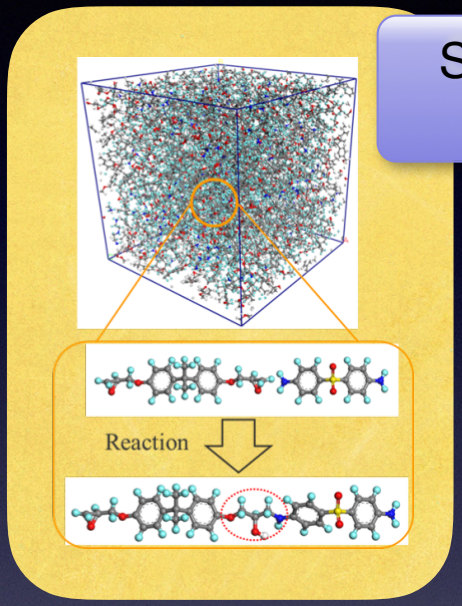
- ★ Network Polymer (thermoset polymer) is a key material for industrial products with carbon composite
  - ✓ high deformation resistance and high durability to extreme environmental conditions
- ★ Its design needs high performance computing for molecular level simulation, up to system level one, such as aircrafts, by using multiscale analysis combined with experiments
  - ✓ Its also needs efficient identification of candidate materials that satisfy the required properties from a plenty of simulation results



Workflow of Polymeric Material Informatics



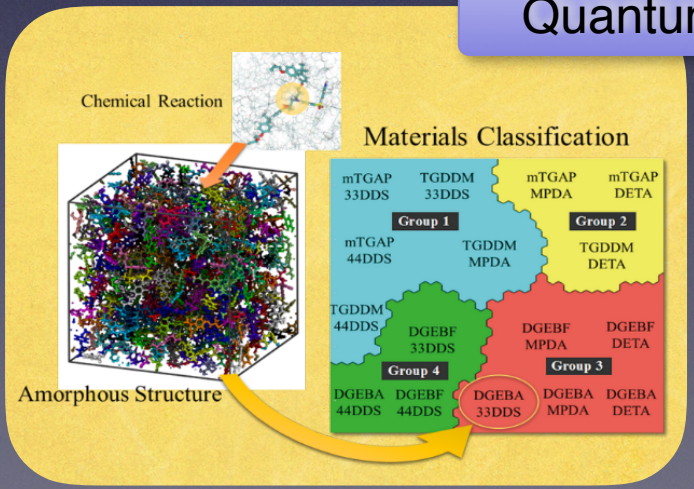
Application Design Approach to Innovative Material Informatics



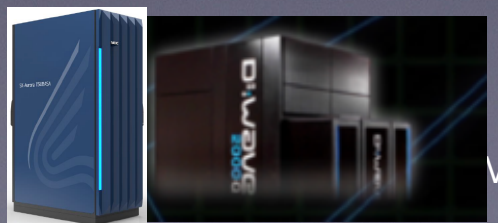
Simulation assisted by next-generation vector-type supercomputing

- ✓More accurate and faster reaction model incorporated into MD simulation for crosslinked network formation in thermosetting resins
- ✓Faster multiscale-simulation for predicting various thermomechanical properties

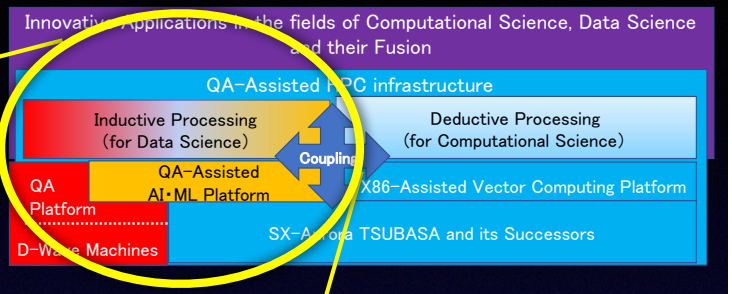
Quantum Annealing-assisted ML frameworks

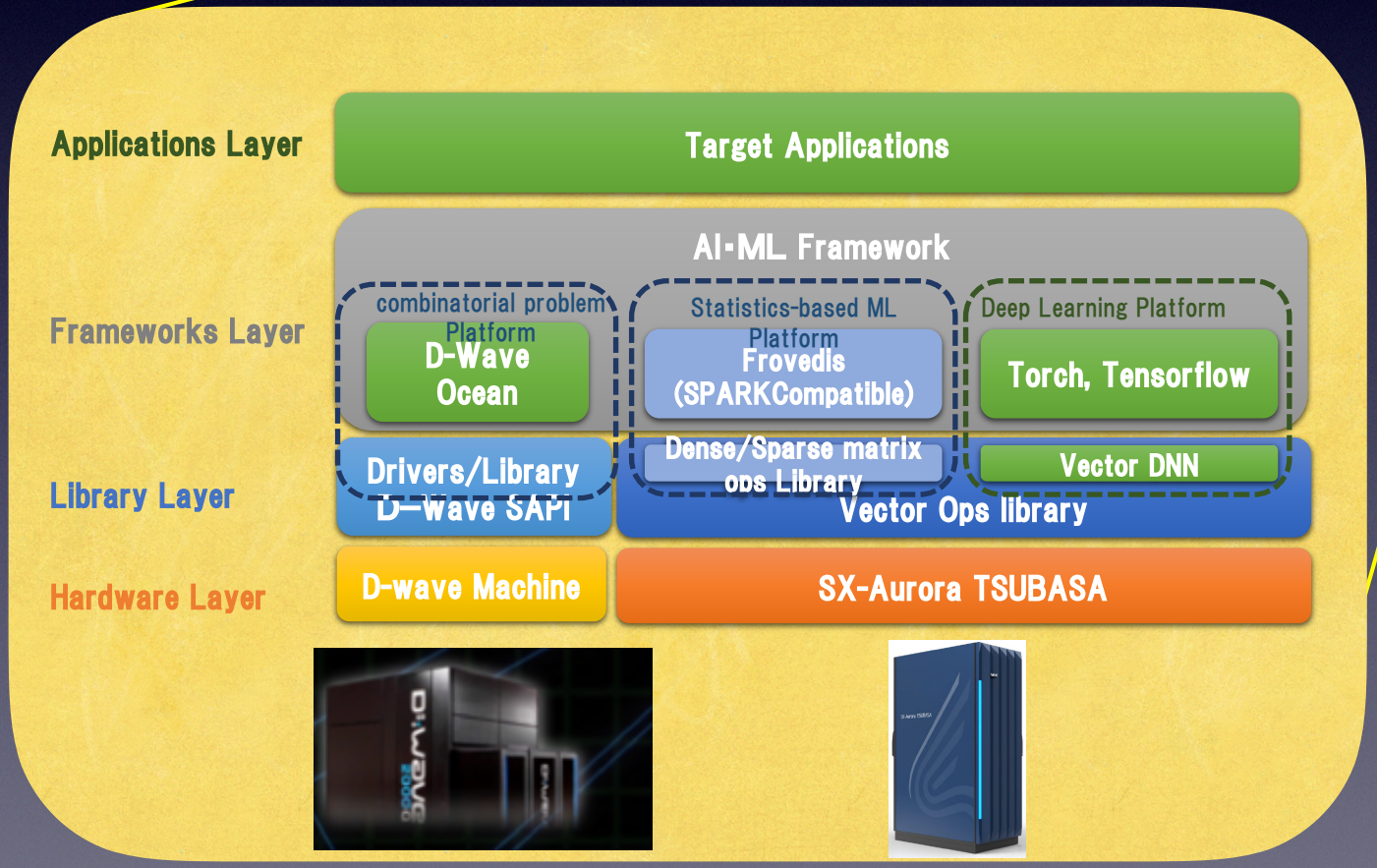


- ✓Hierarchical screening involving clustering approach
- ✓Highly accurate machine learning model based on polymer physics
- ✓Inverse problem-based optimum design for screening of polymeric materials



Closeup View of QA-Assisted AI・ML Platform





Summary

- Emerging applications that integrates high-performance simulation and big-data analysis for the realization of Society 5.0
  - ✓Society 5.0 is a human-centered society that balances economic advancement with the resolution of social problems by a system that highly integrates cyberspace and physical space.
  - ✓Simulation approach and data science approach work in a complementary style to realize Society 5.0.
- Realization of general-purpose computing by ensemble of domain specific architectures as the next generation computing infrastructure toward post Moore's era
  - ✓Maximize computing performance per cost and/or power best suited for a specific domain
  - ✓Best mix of domain specific architectures that satisfies the demands of a wide variety of applications
- ★R&D of a next generation HPC infrastructure: Fusion of Quantum-Annealing and classical HPC in a unified way
  - ✓SX-Aurora TSUBASA, combination of vector engine and X86 engine, has a great potential to achieve a high sustained performance because of its best mix of vector architecture for memory-intensive apps. and x86 architecture for complicated control-intensive apps.
  - ✓D-wave machine, A Quantum annealing machine, is the best domain specific architecture for combinatorial problems.
- ★R&D of three innovative killer apps:
  - ✓real-time optimal Tsunami inundation evaluation planning,
  - ✓digital twin of a power generating Turbine for its effective operation and maintenance, and
  - ✓material informatics for efficient carbon composite products design

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